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October 6, 2004

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
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Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/091,983 03/06/02

Dong Zhong et al.

IMPROVED ULTRA-THIN GATE OXIDE THROUGH POST DECOUPLED PLASMA NITRIDATION ANNEAL

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on October 12, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 10/12/04

This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Action under 1.113 or Notice of Allowance under 1.311 (37CFR 1.97(c)).

I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than 3 months prior to the filing of this statement.

The paper by S.V. Hattangady et al., entitled "Ultrathin nitrogen-profile engineered gate dielectric films," IEDM 96-495, 1996 IEEE, 19.1.1 to 19.1.4, presents a simple and novel scheme for the formation of -4nm gate dielectric films with nitrogen at the top (Gate electrode/dielectric) interface.

The paper by H.N. Al-Shareef et al., entitled "Plasma nitridation of very thin gate dielectrics," Elsevier Science B.V. 2001, Microelectronic Engineering 59(2001), pp. 317-322, compares the performance of NMOSFET devices with nitrided gate oxides using two plasma-based nitridation techniques.

U.S. Patent 6,342,437 to Moore, "Transistor and Method of Making the Same," provides an improved surface P-channel transistor and a method of making the same.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

OIPE 1612 OCT. 14 2004 PATENT & TRADEMARK OFFICE

Docket Number (Optional)	Application Number
CS-01-067	10/091,983
Applicant: Dong Zhong et al.	
Filing Date: 03/06/02	Group Art Unit

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6342437	1/29/02	Moore	438	474	6/1/00

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

- "Ultrathin nitrogen-profile engineered gate dielectric film," by S.V. Hattangady et al., IEDM 96-495, 1996 IEEE, 19.1.1 to 19.1.4.
- "Plasma nitridation of very thin gate dielectrics," Elsevier Science, B.V. 2001, by H.N. Al-Shareef et al., Microelectronic Engineering 59 (2001), pp. 317-322.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.